

Remote Testing Environment

revision v1.1.0

Protectli Flashing Manual



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Introduction

As the new RTE (revision v1.1.0) is now compatible with 1.8V logic levels and the new UART header (J18) has been added (which makes USB/UART external converters not required anymore) it is possible now to flash all the Protectli platforms using only RTE. This document describes the way to connect RTE with the platform that is going to be flashed, proper RTE configuration and a flashing procedure.

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Connections

Serial Debug (COM)

Serial output is provided by RJ45 COM Port. It requires RJ45 to COM cable. RTE Orange Pi should be connected with Ethernet with COM cable. It is necessary to choose whether RS232 DB9 port (J14) or UART header (J18) is enabled for serial communication on RTE by setting jumpers on **UART OUTPUT SELECT** header. For purpose of Protecli flashing DB9 port is used:

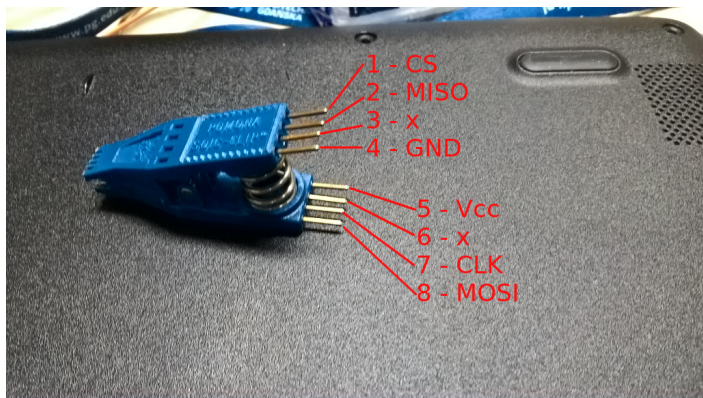
Jumper position (TX and RX)	Serial communication enabled
RS232 + COM	RS232 DB9 port (J14)
EXT + COM	UART header 3.3 V (J18)

SPI

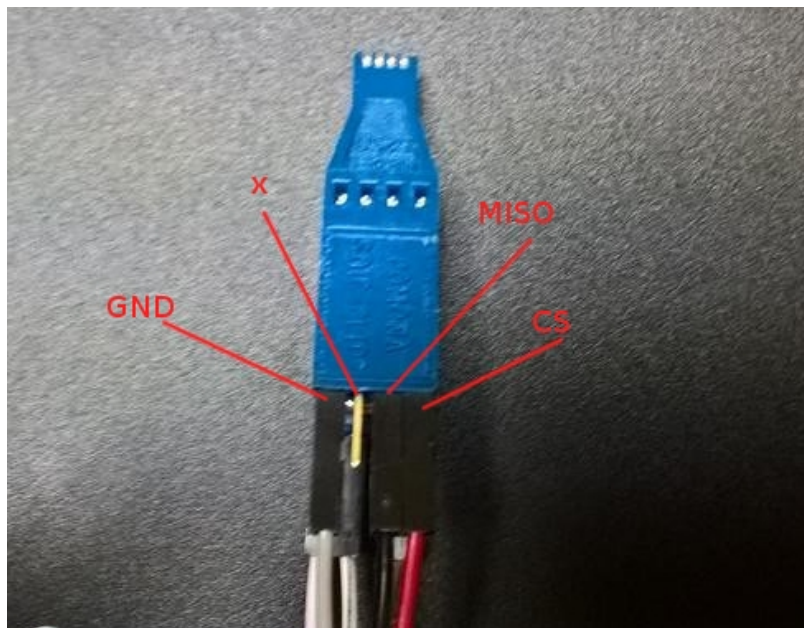
RTE uses J7 header to connect Pomona SOIC clip.

RTE J7	Pomona SOIC clip
Vcc	pin 5 (downside)
GND	pin 4 (upside)
CS	pin 1 (upside)
SCLK	pin 7 (downside)
MISO	pin 2 (upside)
MOSI	pin 8 (downside)

FW2B and FW4B uses [MX25U6435F chip](#) and doesn't provide SPI header. This chip is located on the other side of board, so it isn't possible to use Pomona SOIC clip without removing board from the radiator. FW6B uses MX25L6405D which has the same vendor and package. In this case it is also required to remove board from the radiator. Tests show that idle CPU temperature without radiator stabilizes at 52-58°C (if it is not heavily loaded).



Numbers 1-4 have to be on one side and numbers 5-8 have to be on the other side of clip.





Clip on the chip. Match pin 1 (CS) of the Pomona clip with first pin of SPI chip, marked with small dot engraved on the chip.



Chip on FW2B/FW4B:



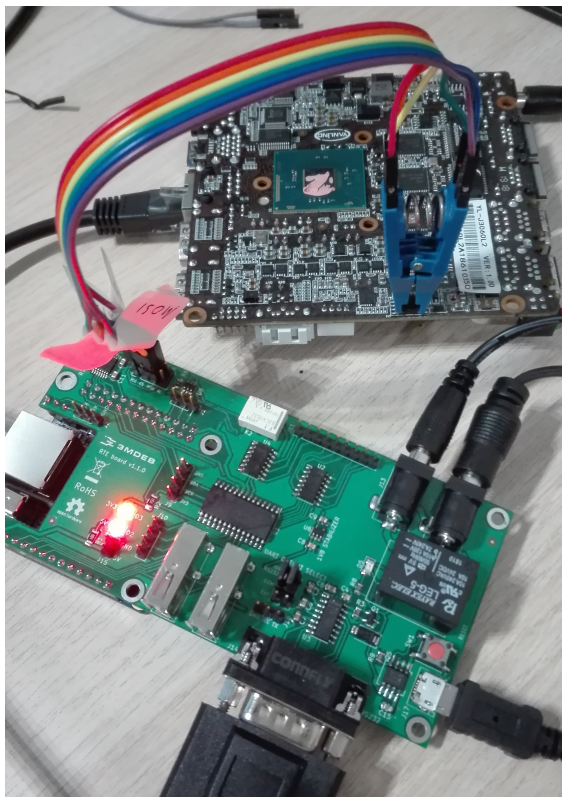


Chip on FW6X platforms:



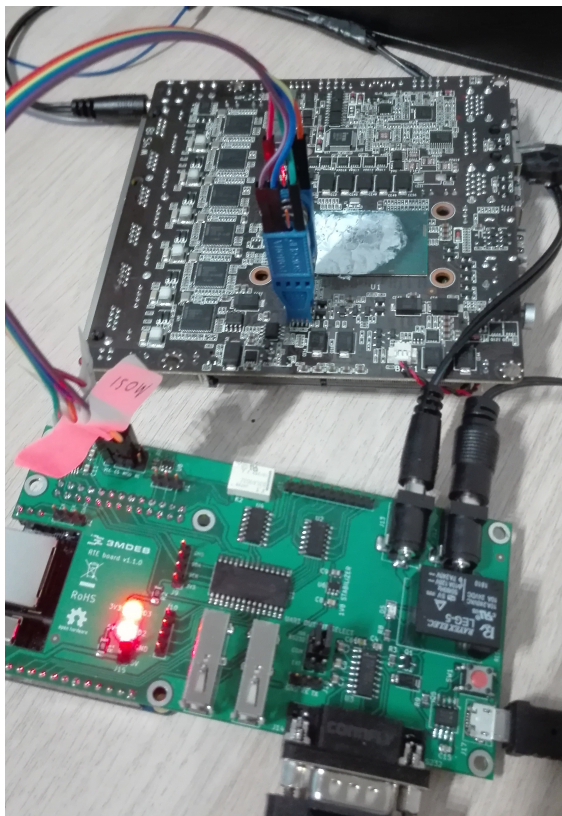


FW2B/FW4B connection:





FW6X platforms connection:



One should be very careful while connecting Pomona. It's easy to accidentally touch other parts of the board, making a short circuit. The best way is to turn the RTE power supply (microUSB connector) when everything is already connected.



Power supply

Connect 12V/4A power supply to RTE J13 connector, then RTE J12 DC Jack – DC Jack power cable to DUT DC connector.

Orange Pi should be powered with 5V/2A DC supply via J17 micro USB header.

RTE configuration

After connecting RTE with the target board, power supply and Ethernet cables, log into Orange Pi in terminal:

```
ssh root@<RTE_IP>
```

i.e.:

```
ssh root@192.168.4.110
```

Orange Pi root password : **meta-rte**

If IP address is unknown, it is also possible to connect RTE with the USB/UART converter using J2 pin header (RX,TX,GND) and then by minicom, or other modem control and terminal emulation program.

MX25U6435F uses 1.8 V logic level for operation, while MX25L6405D uses 3.3 V. It is necessary to adjust Vcc power depending on platform is being flashed.

Enabling/disabling SPI **Vcc**, choosing the voltage level for **Vcc** SPI - either 1.8 or 3.3 V and enabling/disabling SPI lines (some platforms have problems when booting with SPI wires connected) may be controlled by choosing the value of 406,405 and 404 GPIO's.

Enable/disable SPI **Vcc** on demand (this feature is not fully operational yet):

GPIO406 (OC_OUTI) state	SPI Vcc
0 - low	disabled (by default)
1 - high	enabled



Choose the voltage level for **Vcc SPI**:

GPIO405 (OC_OUT2) state	SPI Vcc voltage level
0 - low	1.8 V (by default)
1 - high	3.3 V

Enable/disable SPI lines:

GPIO404 (OC_OUT3) state	SPI lines (MOSI/MISO/CS/SCLK)
0 - low	disabled (by default)
1 - high	enabled

To check these values type:

```
cat /sys/class/gpio/gpio<NR>/value
```

To change these values type:

```
echo <value> > /sys/class/gpio/gpio<NR>/value
```

All above GPIO pins should be configured in Yocto meta-rte system by default (exported and set the **direction** mode to **out**), otherwise one should set up them manually:

```
echo <NR> > /sys/class/gpio/export echo out > /sys/class/gpio/gpio<NR>/direction
```

To flash platform You have to obtain proper firmware image and send it to Orange Pi, i.e. using **scp**.

```
scp <file_path> <user_name>@<ip_adress>:<path_to_file>
```

Then proper voltage level should be set. 1.8 V for FW2B and FW4B, and 3.3 V for FW6X. SPI lines and SPI Vcc should be enabled. Platform should be off during flashing process. This means that GPIO199 should have low (**0**) state.

GPIO199	relay state
0 - low	disabled (power off)
1 - high	enabled (power on)



It's important to carefully connect Pomona to the chip. If it isn't connected precisely enough flashing would not start, because the chip won't be recognized. Before running flashrom gpio pins must be started in the following order: **first gpio 406, then gpio404**. Otherwise flashrom will fail to connect with bios chip.

To flash FW2B or FW4B type:

```
flashrom -f -p linux_spi:dev=/dev/spidev1.0,spispeed=16000 -w <image>
```

i.e.

```
flashrom -f -p linux_spi:dev=/dev/spidev1.0,spispeed=16000 -w  
./protectli_fw2b_v4.9.0.1.rom
```

To flash FW6B type:

```
flashrom -p linux_spi:dev=/dev/spidev1.0,spispeed=16000 -c "MX25L6405D" -w <image> --  
ifd -i bios
```

i.e.

```
flashrom -p linux_spi:dev=/dev/spidev1.0,spispeed=16000 -c "MX25L6405D" -w  
./protectli_fw6_rc5.rom --ifd -i bios
```

In both cases successful flashing shall end with :

```
Reading old flash chip contents... done.  
Erasing and writing flash chip... Erase/write done.  
Verifying flash... VERIFIED.
```



Now Pomona should be disconnected from the platform. The platform is fully operational. If a user want to connect with it via RTE it can be done with **telnet**:

```
telnet <rte_ip> <port>
```

i.e.

```
telnet 192.168.4.110 13541
```

After turning the platform **on** You should enter the boot menu. It can be either done by pressing button on the device, or using RTE connection. One should remember, that the device is powered if the LED indicator on the board is shining and RTE GPIO199 is set to high value. It can be checked with:

```
cat /sys/class/gpio/gpio199/value
```

And changed with

```
echo 1 > /sys/class/gpio/gpio199/value (turn supply ON)
```

```
echo 0 > /sys/class/gpio/gpio199/value (turn supply OFF)
```



Step by Step flashing guide example

- FW2B/FW4B:

```
# Make required connections between RTE and the Vault
# Power On RTE and run locally (with proper IP address):
ssh root@192.168.4.110
password : meta-rte

# relay OFF
echo 0 > /sys/class/gpio/gpio199/value
# SPI Vcc ON
echo 1 > /sys/class/gpio/gpio406/value
# set SPI Vcc to 1.8V
echo 0 > /sys/class/gpio/gpio405/value
# SPI lines ON
echo 1 > /sys/class/gpio/gpio404/value

# start flash command
flashrom -f -p linux_spi:dev=/dev/spidev1.0,spispeed=16000 \
-w ./protectli_fw2b_v4.9.0.1.rom

# Wait until:
Reading old flash chip contents... done.
Erasing and writing flash chip... Erase/write done.
Verifying flash... VERIFIED.

# Disconnect Pomona and power on the board:
echo 1 > /sys/class/gpio/gpio199/value
```

- FW6X:

```
# Make required connections between RTE and the Vault
# Power On RTE and run locally (with proper IP address):
ssh root@192.168.4.110
password : meta-rte

# relay OFF
echo 0 > /sys/class/gpio/gpio199/value
# SPI lines ON
echo 1 > /sys/class/gpio/gpio404/value
# set SPI Vcc to 3.3V
echo 1 > /sys/class/gpio/gpio405/value
# SPI Vcc ON
echo 1 > /sys/class/gpio/gpio406/value

# start flash command
flashrom -p linux_spi:dev=/dev/spidev1.0,spispeed=16000 \
-c "MX25L6405D" -w ./protectli_fw6_rc5.rom --ifd -i bios

# Wait until:
Reading old flash chip contents... done.
Erasing and writing flash chip... Erase/write done.
Verifying flash... VERIFIED.

# Disconnect Pomona and power on the board:
echo 1 > /sys/class/gpio/gpio199/value
```



Troubleshooting

FW6X platforms tend to have problems with the first booting after flashing. If the platform won't bring up, and won't respond to another flashing, One should disconnect the battery from the chip to make it discharge.

One should pull off the marked plug and wait for 15 s.



After that operation the platform will reset several times at the first launch.

This issue doesn't appear if flashing is done via internal programmer.



Additional connection (not required for flashing)

Protectli board has connector with the same pin-out as desktop computers, with PWR_LED, HD_LED, PW_ON and RST. This connector is located in the corner, next to HDMI and SATA ports. Using physical switches temporarily connects signal pin to the ground. Using pin-out described below one can emulate PWR and RST buttons.

RTE	Protectli
J11 pin 9	F_PANEL1 pin 6 (PWR_ON#)
J11 pin 8	F_PANEL1 pin 7 (RST#)
J15 pin 1	F_PANEL1 pin 9 (GND)

It is necessary to use cables adapter 2.54mm to 2.0mm.

Below scripts show basic emulation for pressing power button:

- send power on signal:

```
echo 1 > /sys/class/gpio/gpio410/value
sleep 1
echo 0 > /sys/class/gpio/gpio410/value
```

- send power off signal:

```
echo 1 > /sys/class/gpio/gpio410/value
sleep 5
echo 0 > /sys/class/gpio/gpio410/value
```

For FW6X it is sometimes required to increase `sleep` to 7 seconds.